



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,386	06/19/2001	Son H. Lam	219.40057X00	1333

7590 03/14/2006

Schwegman, Lundberg, Woessner & Kluth P.A.
c/o Anne Richards
1600 TCF Tower
121 S. 8th Street
Minneapolis, MN 55402

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT	PAPER NUMBER
----------	--------------

2116

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4-6 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natu, US. Pat. No. 5,790,850 in view Hrustich et al, US. Pat. No. 4,639,856 (*both references cited in a previous PTO-892*).

3. Claims 1, 6 and 11, Natu teaches a method of a fault resilient booting in a multiprocessor system [*title, abstract*], comprising:

designating one processor as a bootstrap processor [*Step 110 of Fig. 2A, col. 3, lines 44-45*];

testing the bootstrap processor to verify that it will run BIOS code [*col. 3, lines 48-51*];

testing during a POST the operation of said bootstrap processor [*Fig. 2A, col. 3, lines 44-50*];

testing during BIST the operation of said bootstrap processor [*Fig. 2A, col. 3, lines 54-57*];

assigning the bootstrap process to another processor if said bootstrap processor fails a test [*Fig. 2A, col. 3, lines 60-62*];

said steps being implemented in an appliance server management system [*title, abstract*].

Art Unit: 2116

Natu teaches determining if the testing indicates failure [*col. 2, lines 65-66, col. 6, lines 64-65*]. However, Natu fails to teach setting a latch for disabling the failed bootstrap processor if the testing indicates failure.

Hrustich teaches setting a latch disposed within a failing processor to generate an output signal which disables the failing processor [*col. 1, lines 48-53*].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Natu to include setting a latch for disabling bootstrap processor if the testing indicates failure, because if the failing processor has internal failure, it may not be able to operate properly to remove itself from the operation. Thus disabling the failing processor eliminates the problem of relying on a failing processor to perform the appropriate action to remove itself from operation.

4. Claims 4-5, 10, Natu teaches the testing steps are controlled by a controller [*abstract*].

5. Claims 2-3, 7-9, 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natu, US. Pat. No. 5,790,850 in view Hrustich et al, US. Pat. No. 4,639,856 and further in view of Steiert et al, US. Pat. No. 6,122,735 (*cited in a previous office action*).

6. Claims 2, 7-9, 12 and 14, both Natu and Hrustich fail to teach a timer which indicates a failure if it is not reset within a predetermined time period.

Steiert teaches a fault resilient boot circuit [*title, abstract*], comprising a timer [*Timer 300 of Fig 2*]; which indicates a failure if it is not reset within a predetermined time period. [*abstract, col. 3, lines 50-65*];

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Natu to include a timer which indicates a failure if it is not

Art Unit: 2116

reset within a predetermined time period, because it gives the BSP a chance to initialize and begin normal operation [*see Steiert, col. 3, lines 5-11*].

7. Claim 3, Natu teaches a failure in the second or third testing steps also causes said latch to be set [*col. 2, lines 65-66*].

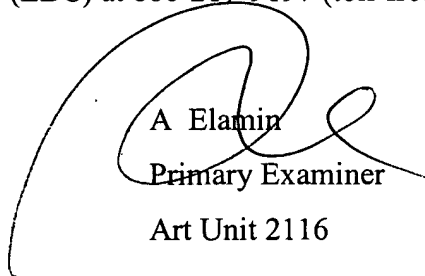
8. Claims 13, 15-16, Natu teaches said first signal is generated when said bootstrap processor fails a POST or a BIST [*Fig. 2A, col. 3, lines 44-65*]; said control unit causes another processor to become the bootstrap processor [*col. 3, lines 44-65*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (571) 272-3674. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



A Elamin
Primary Examiner
Art Unit 2116

March 8, 2006